WHAT IS CLAIMED IS:

1. A method of forming an edge seal along a periphery of an integrated circuit device to provide increased corrosion and oxidation resistance to metallization of the integrated circuit device, the method comprising the steps of:

a. providing a semiconductor substrate having a metallic feature therein;

b. depositing a layer of dielectric material over the semiconductor substrate and metallic feature, the layer of dielectric material comprising a low-k dielectric material;

c. selectively removing a portion of the layer of dielectric material to form a cavity and expose a portion of the metallic feature;

d. conformally depositing a layer of an insulation material in the cavity and over the layer of dielectric material, wherein the insulation material and dielectric material are different materials;

e. removing horizontal portions of the layer of insulation material so as to expose at least the metallic feature in the cavity;

f. depositing a barrier metal on the layer of insulation material in the cavity and on the exposed metallic feature;

g. depositing a high conductivity metal in the cavity to fill the cavity; and

h. planarizing the semiconductor substrate down to the layer of dielectric material.

2. The method of claim 1 wherein the low-k dielectric material comprises SiLK or fluoridized polyimide.

3. The method of claim 1 wherein the layer of dielectric material comprises a bottom layer on the semiconductor substrate, the low-k dielectric material on the bottom layer and a top moisture barrier on the low-k dielectric material.

4. The method of claim 1 wherein the insulation material is selected from the group consisting of SiO_2, SiC, Si_3N4, Al_2O_3, diamond like carbon, polyimide and combinations thereof.

5. The method of claim 1 wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium, titanium nitride, tungsten silicide and combinations thereof.

6. The method of claim 1 wherein the high conductivity metal is copper.

7. The method of claim 1 wherein the thickness of the insulation material in the cavity is 0.05 microns to 0.5 microns.

8. The method of claim 1 wherein the cavity comprises at least two contiguous cavities which form a damascene structure.

9. An edge seal around the periphery of an integrated circuit device comprising:

a. a semiconductor substrate;

b. a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material;

c. a metallic wall of a high conductivity metal in the layer of dielectric material; and

d. a layer of insulation material between the metallic wall and the dielectric material, wherein the insulation material and dielectric material are different materials.

10. The edge seal of claim 9 wherein the low-k dielectric material comprises SiLK or fluoridized polyimide.

11. The edge seal of claim 9 wherein the layer of dielectric material comprises a bottom layer on the semiconductor substrate, the low-k dielectric material on the bottom layer and a top moisture barrier on the low-k dielectric material.

12. The edge seal of claim 9 wherein the insulation material is selected from the group consisting of SiO_2, SiC, Si_3N4, Al_2O_3, diamond like carbon, polyimide and combinations thereof.

13. The edge seal of claim 9 further comprising a barrier layer between the metallic wall and the insulation material wherein the barrier layer is selected from the group

consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium, titanium nitride, tungsten silicide and combinations thereof.

14. The edge seal of claim 9 wherein the high conductivity metal is copper.

15. The edge seal of claim 9 wherein the thickness of the insulation material is 0.05 microns to 0.5 microns.

16. The edge seal of claim 9 wherein there are two metallic walls in the at least one layer of dielectric material and there is a layer of insulation material between the dielectric material and each of the metallic walls with each layer of insulation material being of a different material than the dielectric material.

17. A method of forming an edge seal along a periphery of an integrated circuit device to provide increased corrosion and oxidation resistance to metallization of the integrated circuit device, the method comprising the steps of:

a. providing a semiconductor substrate having a metallic feature therein;

b. depositing a layer of dielectric material over the semiconductor substrate and metallic feature, the layer of dielectric material comprising a low-k dielectric material;

c. selectively removing a portion of the layer of dielectric material to form two first cavities and expose a portion of the metallic feature;

d. depositing an insulation material to fill the two first cavities, wherein the insulation material and dielectric material are different materials;

e. selectively removing a portion of the layer of dielectric material, and any overlying insulation material to form a second cavity;

f. depositing a barrier metal in the second cavity and on the exposed metallic feature;

g. depositing a high conductivity metal in the second cavity to fill the cavity; and

h. planarizing the semiconductor substrate down to the layer of dielectric material.

18. An edge seal around the periphery of an integrated circuit device comprising:

a. a semiconductor substrate;

b. a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material;

c. a metallic wall in the layer of dielectric material; and

d. a wall of insulation material between the metallic wall and the periphery of the integrated circuit device wherein the insulation material and dielectric material are different materials.